On a Realization of Multi-terminal Universal Interconnection Networks using Contact Switches

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Abstract—A universal interconnection network implements arbitrary interconnections among n terminals. This paper considers a problem to realize such a network using contact switches. When $n = 2$, it can be implemented with a single switch. The number of different connections among n terminals is given by the Bell number $B(n)$. The Bell number shows the total number of methods to partition n distinct elements. For $n = 2, 3, 4, 5$ and 6, the corresponding Bell numbers are $2, 5, 15, 52$, and 203, respectively. This paper shows a method to realize an n terminal universal interconnection network with $\frac{3}{8}(n^2-1)$ contact switches when $n = 2m + 1 \geq 5$, and $\frac{n}{8}(3n + 2)$ contact switches, when $n = 2m \geq 6$. Also, it shows a lower bound on the number of contact switches to realize an n-terminal universal interconnection network.

Index Terms—interconnection network, partition number, Bell number, complexity of circuits, contact switch, multi-position switch, universal network, contact network

I. INTRODUCTION

Problem 1.1: Consider a controller of a solar energy system consisting of the following seven units:

1) Solar panel 1
2) Solar panel 2
3) Rechargeable battery unit 1
4) Rechargeable battery unit 2
5) Load unit 1
6) Load unit 2
7) Voltage meter unit

We need to change the interconnections among these units depending on various conditions. What kind of network should be used to allow necessary connections?

This problem can be solved by using a universal interconnection network among seven terminals.

In this paper, we show that to implement an n-terminal universal interconnection network, $\frac{3}{8}(n^2-1)$ contact switches when $n = 2m + 1 \geq 5$, and $\frac{n}{8}(3n + 2)$ contact switches, when $n = 2m \geq 6$, are sufficient. The rest of this paper is organized as follows: Section II introduces terminology used in this paper. Section III shows a method to realize a universal interconnection network. Section IV shows a realization of universal interconnection network using multi-position switches. Section V concludes the paper, and shows future problems. And, Section VI surveys related research.

II. DEFINITIONS AND BASIC PROPERTIES

This section defines terminology used in this paper.
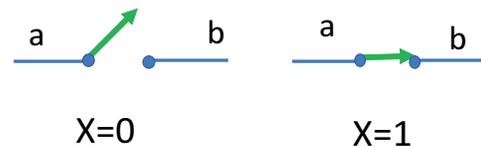
Fig. 2.1. Contact Switch

Definition 2.1: Fig. 2.1 shows a **contact switch**. When $x = 0$, the terminal a is disconnected from the terminal b. When $x = 1$, the terminal a is connected to the terminal b. It is also called a **single-pole single-throw switch**.

A contact switch can be implemented by a magnetic relay [13], [9], MEMS, or semiconductors.

A contact switch is **bidirectional**, i.e, the terminals connected together have the same electrical potential. Thus, an analog signal can be transmitted. Since only contact switches are used in this paper, a contact switch is simply called a **switch**.

Definition 2.2: A **partition** of a set S is a set of non-null subsets of S. Each element in S belongs to exactly one of these subsets. An element of a partition is called a **block**.

Example 2.1: The set $S = \{1, 2\}$ has two partitions: $\{[1], [2]\}$ and $\{[1, 2]\}$.

Example 2.2: The set $S = \{1, 2, 3\}$ has five partitions: $\{[1], [2], [3]\}$, $\{[1, 2], [3]\}$, $\{[1, 3], [2]\}$, $\{[1], [2, 3]\}$, and $\{[1, 2, 3]\}$.

Example 2.3: The set $S = \{1, 2, 3, 4\}$ has the following 15 partitions: $\{[1], [2], [3], [4]\}$, $\{[1, 2], [3], [4]\}$, $\{[1, 3], [2], [4]\}$, $\{[1], [2, 3], [4]\}$, $\{[1, 2, 3], [4]\}$, $\{[1, 4], [2], [3]\}$, $\{[1, 2, 4], [3]\}$, $\{[1, 3, 4], [2]\}$, $\{[1, 4], [2, 3]\}$, $\{[1, 2, 3, 4]\}$, $\{[1], [2, 4], [3]\}$, $\{[1, 3], [2, 4]\}$, $\{[1], [2, 3, 4]\}$, $\{[1], [2], [3, 4]\}$, and $\{[1, 2], [3, 4]\}$.

Definition 2.3: The number of partitions of a set of n distinguishable elements into non-empty, indistinguishable boxes is the **Bell number**. It is denoted by $B(n)$.

Table 2.1 shows the values of $B(n)$ for $n = 2, 3, \ldots, 8$.

The n-th Bell number $B(n)$ is given by the following recurrence relation [4]:

$$B(n + 1) = \sum_{k=0}^{n} \binom{n}{k} B(k).$$

n	$B(n)$
2	2
3	5
4	15
5	52
6	203
7	877
8	4140
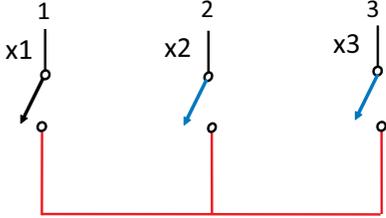
Fig. 3.1. Three-terminal Universal Interconnection Network $U(3)$

Fig. 3.2. Realization of a $(k+1)$-terminal Universal Interconnection Network

Definition 2.4: An **n-terminal universal interconnection network** $U(n)$ realizes arbitrary interconnections among n terminals. It realizes $B(n)$ different connection patterns.

III. REALIZATION OF UNIVERSAL INTERCONNECTION NETWORKS

A. Upper Bound on the Number of Switches

Lemma 3.1: A 3-terminal universal interconnection network $U(3)$ can be realized with three switches.

(Proof) Consider the circuit in Fig. 3.1. It shows the state where all the switches are in the *open* states. This state is selected when the control inputs are $(x_1, x_2, x_3) = (0, 0, 0)$. In this state, all the terminals are isolated. In this case, the network realizes the partition $\{[1], [2], [3]\}$. For other states can be realized as shown in Table 3.1. □

TABLE 3.1
COMBINATION TABLE FOR $U(3)$

$Class$	x_1	x_2	x_3	Partition
1	0	0	0	[1], [2], [3]
2	1	1	0	[1, 2], [3]
3	1	0	1	[1, 3], [2]
4	0	1	1	[1], [2, 3]
5	1	1	1	[1, 2, 3]

Lemma 3.2: A $(k + 1)$-terminal universal interconnection network $U(k + 1)$ can be realized by connecting k switches to the k-terminal universal interconnection network $U(k)$, as shown in Fig. 3.2.

(Proof) Assume that $U(k)$ can realize any partition of k elements.

We can append the $(k+1)$-th element to an arbitrary block of a partition of k elements, by setting one of the switches to the *closed* position as shown in Fig. 3.2. Also, by setting all the switches to the *open* positions, we can make the $(k + 1)$-th element isolated. In this way, all the partitions of $k + 1$ elements are realized. □

Theorem 3.1: An n-terminal universal interconnection network $U(n)$ can be realized with $C_1(n) = \frac{n(n-1)}{2}$ switches.

(Proof) We use mathematical induction on the number of terminals n.

- When $n = 2$, $U(2)$ can be realized with $C_1(2) = 1$ switch.
- When $n = 3$, $U(3)$ can be realized with $C_1(3) = 3$ switches, by Lemma 3.1.
- Assume that a k-terminal universal interconnection network $U(k)$ can be realized with $C_1(k) = \frac{k(k-1)}{2}$ switches. By Lemma 3.2, a $(k + 1)$-terminal universal interconnection network $U(k + 1)$ can be realized by connecting k switches to $U(k)$.
- Let $C_1(k + 1)$ be the sufficient number of switches to realize $U(k+1)$. Then, $C_1(k+1)$ satisfies the following relation:

$$C_1(k + 1) = C_1(k) + k.$$

By solving this recurrence relation, we have

$$C_1(k + 1) = \frac{(k + 1)k}{2}.$$

- Hence, we have the theorem.

□

Lemma 3.3: A five-terminal universal interconnection network $U(5)$ can be realized with nine switches.

(Proof) Consider the network shown in Fig. 3.3. Let us introduce **ternary signals** X_i ($i = 1, 2, 3, 4, 5$) that control the connections among terminals. Also consider the **three-position switch** [8] shown in Fig. 3.4. This switch works as follows: When $X_i = 0$, the common armature is connected to the upper contact a; when $X_i = 1$, the common armature is connected to the middle contact b; and when $X_i = 2$, the common armature is connected to the lower contact network c.
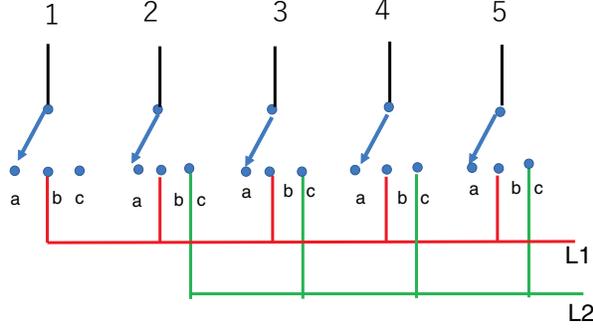
Fig. 3.3. Five-terminal Universal Interconnection Network $U(5)$
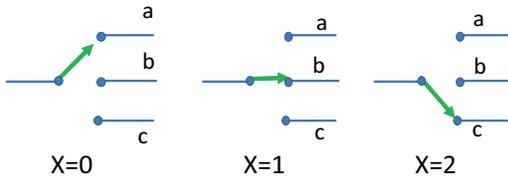
Fig. 3.4. Three-position Switch

In the network, each terminal i is connected to no bus line when $X_i = (0,0)$; to $L1$ (the red bus line) when $X_i = (0,1)$; and to $L2$ (the green bus line) when $X_i = (1,0)$.

By setting the values of X_i as shown in Table 3.2, we can realize all 52 different partitions.

Note that the three-position switch for terminal 1 can be replaced by a switch. Also, each of the three-position switches for terminals 2 to 5 can be replaced by a pair of switches. In Fig. 3.3, contacts a for three-position switches are isolated, so no switch is necessary for the contacts a. Thus, the circuit can be implemented by nine switches. □

Note that when $n = 5$, Theorem 3.1 gives $C_1(5) = 10$. However, the realization shown in Fig. 3.3 requires only nine switches, and thus requires fewer switches. Bus lines are used to implement blocks with more than two elements, such as [1,2] and [3,4,5]. With this, when $n \geq 5$, the upper bound of Theorem 3.1 can be reduced by one.

Theorem 3.2: An n-terminal universal interconnection network $U(n)$ can be realized with $C_2(n) = \frac{(n+1)(n-2)}{2}$ switches when $n \geq 5$.

(Proof)
- We use mathematical induction on the number of terminals n.
- When $n = 5$, $U(5)$ can be realized with $C_2(5) = 9$ switches by Lemma 3.3.
- Similarly to the proof of Theorem 3.1, by solving the recurrence relation $C_2(k+1) = C_2(k) + k$ and $C_2(5) = 9$, we have $C_2(k+1) = \frac{(k+2)(k-1)}{2}$.

□

TABLE 3.2
COMBINATION TABLE FOR $U(5)$

Class	X_1	X_2	X_3	X_4	X_5	Partition
1	0	0	0	0	0	[1],[2],[3],[4],[5]
2	1	1	0	0	0	[1,2],[3],[4],[5]
3	1	0	1	0	0	[1,3],[2],[4],[5]
4	1	0	0	1	0	[1,4],[2],[3],[5]
5	1	0	0	0	1	[1,5],[2],[3],[4]
6	0	1	1	0	0	[2,3],[1],[4],[5]
7	0	1	0	1	0	[2,4],[1],[3],[5]
8	0	1	0	0	1	[2,5],[1],[3],[4]
9	0	0	1	1	0	[3,4],[1],[2],[5]
10	0	0	1	0	1	[3,5],[1],[2],[4]
11	0	0	0	1	1	[4,5],[1],[2],[3]
12	1	1	2	2	0	[1,2],[3,4],[5]
13	1	1	2	0	2	[1,2],[3,5],[4]
14	1	1	0	2	2	[1,2],[4,5],[3]
15	1	2	1	2	0	[1,3],[2,4],[5]
16	1	2	1	0	2	[1,3],[2,5],[4]
17	1	0	1	2	2	[1,3],[4,5],[2]
18	1	2	2	1	0	[1,4],[2,3],[5]
19	1	2	0	1	2	[1,4],[2,5],[3]
20	1	0	2	1	2	[1,4],[3,5],[2]
21	1	2	2	0	1	[1,5],[2,3],[4]
22	1	2	0	2	1	[1,5],[2,4],[3]
23	1	0	2	2	1	[1,5],[3,4],[2]
24	0	1	1	2	2	[2,3],[4,5],[1]
25	0	1	2	1	2	[2,4],[3,5],[1]
26	0	1	2	2	1	[2,5],[3,4],[1]
27	0	1	2	1	2	[3,5],[2,4],[1]
28	0	1	1	2	2	[4,5],[2,3],[1]
29	1	1	1	2	2	[1,2,3],[4,5]
30	1	1	2	1	1	[1,2,4],[3,5]
31	1	1	2	2	1	[1,2,5],[3,4]
32	1	2	1	1	2	[1,3,4],[2,5]
33	1	2	2	1	2	[1,3,5],[2,4]
34	1	2	2	2	1	[1,4,5],[2,3]
35	1	2	2	2	1	[2,3,4],[1,5]
36	1	2	2	1	2	[2,3,5],[1,4]
37	1	1	2	2	2	[3,4,5],[1,2]
38	1	1	1	0	0	[1,2,3],[4],[5]
39	1	1	0	1	0	[1,2,4],[3],[5]
40	1	1	0	0	1	[1,2,5],[3],[4]
41	1	0	1	1	0	[1,3,4],[2],[5]
42	1	0	1	0	1	[1,3,5],[2],[4]
43	1	0	0	1	1	[1,4,5],[2],[3]
44	0	1	1	1	0	[2,3,4],[1],[5]
45	0	1	1	0	1	[2,3,5],[1],[4]
46	0	0	1	1	1	[3,4,5],[1],[2]
47	1	1	1	1	0	[1,2,3,4],[5]
48	1	1	1	0	1	[1,2,3,5],[4]
49	1	1	0	1	1	[1,2,4,5],[3]
50	1	0	1	1	1	[1,3,4,5],[2]
51	0	1	1	1	1	[2,3,4,5],[1]
52	1	1	1	1	1	[1,2,3,4,5]

B. Lower Bound on the Number of Switches

Lemma 3.4: To realize $U(n)$, at least $\lceil \log_2 B(n) \rceil$ switches are necessary, where $B(n)$ denotes the Bell number.

As for Bell numbers, the following result is known [3].

Lemma 3.5: For every $\varepsilon > 0$, there exists an integer $n_0 = n_0(\varepsilon)$ such that for all $n > n_0$,

$$\left(\frac{n}{e \ln n} \right)^n < B(n).$$

From this, we have the following:

Theorem 3.3: To realize $U(n)$, at least

$$O(n \log n - n \log \log n)$$

switches are necessary.

IV. REALIZATION USING MULTI-POSITION SWITCHES

In the previous section, three-position switches were used to realize a universal interconnection network $U(5)$. In this

TABLE 4.1
PARTITION NUMBERS $P(n)$

n	$P(n)$
2	2
3	3
4	5
5	7
6	11
7	15
8	22

Fig. 4.1. Six-terminal Universal Interconnection Network $U(6)$

section, we show a method to realize a large-scale network with multi-position switches and bus lines.

Lemma 4.1: A six-terminal universal interconnection network $U(6)$, can be realized with six four-position switches.

(Proof) We show that Fig. 4.1 realizes an arbitrary partition of six elements. In the upper part of this figure, six **four-position switches** are used. The operation of a four-position switch shown in Fig. 4.2 is as follows: When $X = 0$, the common armature is connected to the contact a; when $X = 1$, the common armature is connected to the contact b; when $X = 2$, the common armature is connected to the contact c; and when $X = 3$, the common armature is connected to the contact d.

The number of partitions of distinct $n = 6$ elements is $B(6) = 203$. Note that the set of partitions has a **symmetric property**, That is, a partition is realized by a network, then the partition that is obtained by any permutation of the variables, is also realized by the same network.

For example, suppose that Fig. 4.1 realizes the partition

$$\{[1, 2], [3, 4], [5, 6]\},$$

then the partition

$$\{[1, 6], [2, 5], [3, 4]\},$$

is also realized by the same network, when x_1, x_6, x_2, x_5, x_3 and x_4 are connected to the terminals 1, 2, 3, 4, 5 and 6, respectively.

Thus, the number of partitions to consider is reduced to the number of partitions of eight indistinguishable elements.

In general, the number of partitions of n indistinguishable elements is called the **partition number**[1], and is denoted by $P(n)$ [2]. Table 4.1 shows $P(n)$ for up to $n = 8$.

To prove the lemma, it is sufficient to show that all $P(6) = 11$ partitions shown in the second column of Table 4.2 are realized.

As shown in the last six columns of Table 4.2, by setting the values to the variables X_i $(i = 1, 2, \ldots, 6)$, we can realize all 11 partitions. Here, when the value of variable X_i is $j > 0$, the terminal i is connected to the bus line L_j. While, when the value of the variable X_i is equal to 0, the terminal is isolated. Note that Fig. 4.1 shows the state where all the variables X_i are zeros. From these, we have the lemma. $\square$

In Fig.4.1, replace each four-positional switch with the circuit in Fig. 4.3, and we have $U(6)$ with $6 \times 3 = 18$

[1]Ferrers diagram or Young diagrams can be used to derive this number.
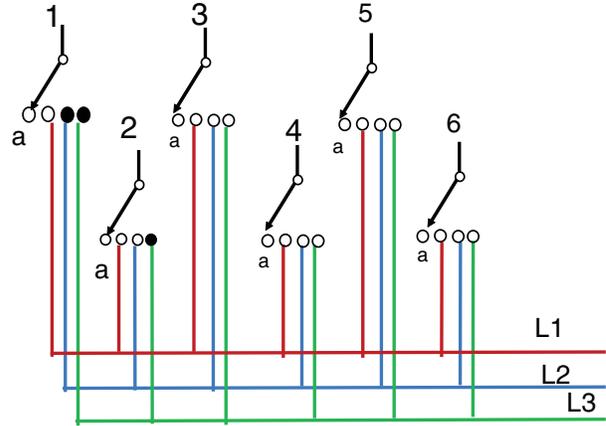
switches. In Fig. 4.1, contacts a are isolated. Thus, no switch is necessary for the contacts a.
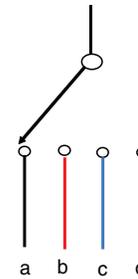
Fig. 4.2. Four-position Switch
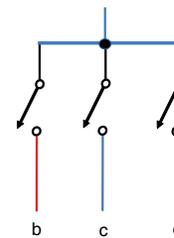
Fig. 4.3. Realization of a Four-position Switch

Lemma 4.2: When $n = 2m$ and $m \geq 3$, an n-terminal universal interconnection network $U(n)$ can be realized with n $(m + 1)$-position switches.

(Proof) Consider the network which is a generalized version of $U(6)$ in Fig. 4.1. Assume that the number of terminals is $n = 2m$, the number of bus lines is m, and in each column,

there is a $(m+1)$-position switch. In this case, the generalized network realizes an arbitrary partition. □

Theorem 4.1: When $n = 2m$ and $n \geq 6$, an n-terminal universal interconnection network $U(n)$ can be realized with

$$C_3(n) = \frac{m}{2}(3m+1) = \frac{n}{8}(3n+2)$$

switches.

(Proof) First, realize an n-terminal universal interconnection network $U(n)$ using n $(m+1)$-position switches, by Lemma 4.2. Then, replace each $(m+1)$-position switch with m switches. In this case, the total number of switches is

$$2m \times m = 2m^2.$$

However, we can remove redundant switches. In Fig. 4.1, we can remove the three contacts with black circles. This can be done using the strategy: A terminal with the smaller index uses the bus line with the smaller index.

So, the terminal 1 can be connected to only the bus line $L1$. Also, the terminal 2 can be connected to the bus line $L1$ or $L2$. With this method, we can remove

$$(m-1) + (m-2) + \cdots + 2 + 1 = \frac{m(m-1)}{2}$$

switches. Thus, the total number of switches is

$$2m^2 - \frac{m(m-1)}{2} = \frac{m}{2}(3m+1).$$

□

Note that when $n = 6$, $C_1(6) = C_3(6) = 15$, and $C_2(6) = 14$. However, when $n = 8$, $C_1(8) = 28$, $C_2(8) = 27$, and $C_3(8) = 26$ [2].

Similarly, we have the following result.

Theorem 4.2: When $n = 2m + 1$ and $n \geq 5$, an n-terminal universal interconnection network $U(n)$ can be realized with

$$C_3(n) = \frac{3}{2}m(m+1) = \frac{3}{8}(n^2 - 1)$$

switches.

A design method for $U(n)$ is summarized as:

Algorithm 4.1:
1) Make a combination table for $U(n)$ such as Table 3.1 and Table 3.2.
2) Prepare $\lfloor \frac{n}{2} \rfloor$ bus lines.
3) Prepare n $\lfloor \frac{n}{2} \rfloor$-position switches.
4) Connect the terminals and bus lines according to the combination table.
5) Replace the multi-position switches with simple switches.
6) Remove redundant switches.

Definition 4.1: Let $C(n)$ be the minimum number of switches to realize an n terminal universal interconnection network $U(n)$.

From Lemmas 3.1 and 3.3, and Theorems 3.1, 3.2, 4.1, and 4.2, we have the following:

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[2] C_1 denotes the upper bound derived from Theorem 3.1, C_2 denotes the upper bound derived from Theorem 3.2, and C_3 denotes the upper bound derived from Theorems 4.1 and 4.2.

TABLE 4.2
REALIZATION OF $U(6)$ USING FOUR-POSITION SWITCHES

Class	Partition	X_1	X_2	X_3	X_4	X_5	X_6
1	[1], [2], [3], [4], [5], [6]	0	0	0	0	0	0
2	[1,2], [3], [4], [5], [6]	1	1	0	0	0	0
3	[1,2,3], [4], [5], [6]	1	1	1	0	0	0
4	[1,2], [3,4], [5], [6]	1	1	2	2	0	0
5	[1,2,3,4], [5], [6]	1	1	1	1	0	0
6	[1,2,3], [4,5], [6]	1	1	1	2	2	0
7	[1,2], [3,4], [5,6]	1	1	2	2	3	3
8	[1,2,3,4,5], [6]	1	1	1	1	1	0
9	[1,2,3,4], [5,6]	1	1	1	1	2	2
10	[1,2,3], [4,5,6]	1	1	1	2	2	2
11	[1,2,3,4,5,6]	1	1	1	1	1	1

Corollary 4.1:

$$
\begin{aligned}
C(2) &= 1, \\
C(3) &= 3, \\
C(4) &\leq 6, \\
C(5) &\leq 9, \\
C(6) &\leq 14, \\
C(n) &\leq \frac{3}{8}(n^2 - 1), (n = 2m+1, n \geq 5) \\
C(n) &\leq \frac{n}{8}(3n+2), (n = 2m, n \geq 6)
\end{aligned}
$$

V. CONCLUDING REMARKS

In this paper, we showed a method to realize an n-terminal universal interconnection network using $\frac{n}{8}(3n+2)$ contact switches, when $n = 2m \geq 6$, and $\frac{3}{8}(n^2 - 1)$ contact switches, when $n = 2m+1 \geq 5$.

These switches can be controlled by **multi-valued signals** X_i $(i = 1, 2, \ldots, n)$, shown, for example, in Tables 3.2 and 4.2. The design of such a circuit is a future problem.

The problem that appeared in the introduction can be solved by Theorem 4.2. We can use at most $C_3(7) = 18$ switches. In many cases, only a proper subset of $B(7) = 877$ different connections is used. Thus, the number of necessary switches can be less than 18. Given the necessary connection patterns, the minimization of switches is a future problem.

VI. RELATED WORK

Pioneering work on two-terminal contact networks was started by Nakashima [14] and Shannon [17].

The upper and lower bounds on the number of switches to realize an arbitrary logic function were derived by Shannon [18].

Minimization on the number of switches to realize a given logic function using a series-parallel network was considered by Lawler [12].

As for n-terminal interconnection networks, Harrison [10] showed a method to analyze the transmission functions using transitive closure of the connection matrix.

Consider the case with two groups of n terminals, where one terminal in a group is connected to exactly one terminal in the other group. Since such networks are frequently used

in telephone exchange networks, many papers have been published [6], including **non-blocking minimal spanning switch** [7].

A realization of transmission function using a lattice of four-terminal switches was considered in [1].

As for hardware that generates all possible partitions, Butler and Sasao [5] showed an FPGA realization. This circuit generates all partitions (for example, the last column of Table 3.2), but is not an interconnection network.

As for three-terminal networks, Koga [11] showed various logic circuits, but they are **unidirectional** networks.

A **universal logic module** realizes an arbitrary n-variable logic function. It can be implemented by a logic network with $m \simeq O(2^n / \log n)$ inputs. Since it is quite important, many papers have been published [19].

However, within the authors knowledge, no paper on universal interconnection network has been published.

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