Remarks on the Design of First Digital Computers in Japan - Contributions of Yasuo Komamiya

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Abstract. This paper presents some less known details about the work of Yasuo Komamiya in development of the first relay computers using the theory of computing networks that is based on the former work of Oohashi Kan-ichi and Mochiori Goto at the Electrotechnical Laboratory (ETL) of Agency of Industrial Science and Technology, Tokyo, Japan. The work at ETL in the same direction was performed under guidance of Mochinori Goto.

Keywords: Digital computers · Relay-based computers · Parametron computers · Transistorised computers · History · Arithmetic circuits

1 Introduction

In the first half of the 20th century, many useful algorithms were developed to solve various problems in different areas of human activity. However, most of them require intensive computations, due to which their applications, especially wide applications, have been suppressed by the lack of the corresponding computing devices. Even before that, already in late thirties, it was clear that discrete and digital devices are more appropriate for such applications that require complex computations. Therefore, in fifties of the 20th century, the work towards development of digital computers was a central subject of research at many important national level institutions. This research was performed equally in all technology leading countries all over the world, notably USA, Europe, and Japan.

In this paper, we briefly discuss the work in this area performed in Japan at the Electrotechnical Laboratory (ETL), Agency of Industrial Science and Technology, conducted by Mochinori Goto, and in particular we present some

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less known details about the work of Yasuo Komamiya and his contributions in the development of the first relay computers based on the theory of computing networks [4–6] by elaborating the results of Mochinori Goto and Oohashi Kan-ichi, the actual at that time and the former director of ETL.

2 Professional Biography of Yasuo Komamiya

In September 1944, Yasuo Komamiya graduated from the School of Engineering of Tokyo Imperial University, Tokyo, Japan in the area of electrical engineering. During his study, he attended courses of Mochinori Goto, who was at the same time the Director of the Electrotechnical Laboratory (ETL) of Agency of Industrial Science and Technology, Japan, which was important for his further professional work and development as will be discussed below. Within this course, Komamiya got the subject for his research leading to a theory of computing networks due to which Komamiya was awarded by the degree of PhD in engineering from Tokyo Imperial University.

In November 1944, Komamiya joined the Basic Research Division of the ETL as an engineer. Starting from January 1957, he spent a year at the Computation Laboratory of Harvard University, which was at that time led by Howard Aiken who was championing the application of arithmetic expressions for Boolean functions to describe and design arithmetic circuits. By expanding his research interest, from September 1962, he stayed for a year at the Digital Computation Laboratory, University of Illinois working in coding theory.

Komamiya stayed with ETL until 1980, by holding different positions including the Head of Applied Mathematics, Department of Physics Division, the Division Director of Control Systems Research, Director of Electronic Components (Devices) Research. From 1980 to 1986 he was a Professor at the Graduate School of Integrated Science and Technology, Kyushu University in Fukuoka. After retirement in 1986, Komamiya was appointed as a Professor of Meiji University in Kanagawa where he worked until 1993.

Figure 1 shows a photo of Komamiya (central figure) with associates.

3 Theory of Computing Networks

The work towards the first computers in Japan is strictly related to the Electrotechnical Laboratory (ETL) of the Japanese government that was established by the Ministry of Communication of Japan in 1891. In 1948, ETL was reorganised into two units, the ETL conducting research on power engineering and power electronic, and the Electrical Communication Laboratory performing research in communication and electronic engineering including design of computing devices and development of the first computers. The underlined theoretical framework can be traced as follows. Oohashi Kan-ichi, who served as the Director of ETL until 1945, developed a theory of electric relay circuits by taking into account the delay in functioning of electric relays. This theory required solving a functional equation that depends on time as an explicit variable. The problem of solving this

Fig. 1. From left to the right Tsutomu Sasao, Teruhiko Yamada, Yasuo Komamiua, Yoshihiro Iwadare, and an associate whose name is not recorded.

functional equation was explored further by Mochinori Goto, who was appointed as the Director of Power Engineering Research Division, and further promoted into the General Director of ETL in 1952. Goto solved the problem initiated by Oohashi by expanding the Boolean algebra by modeling the relay delay time as a logic function, which enables modeling behaviour of relay circuits as a function depending on time by solving an equation including an unknown logic function [1–3]. The theory called by Goto *Logical Mathematics* permitted to analyze and design relay circuits via calculations. The work of Goto was reviewed by Alonzo Church in *The Journal of Symbolic Logic*, Vol. 20, No. 3, 1955, 285–286.

This theory implemented by Yasuo Komamiya become a mathematical foundation for constructing computing networks [4,6]. In several publications from 1951 to 1959, Yasuo Komamiya discussed the theoretical foundations for converting the design of computing networks from an engineering discipline into a subdiscipline of applied mathematics [4–10].

In the case of adders, the chief idea is to represent the sum of natural numbers in terms of binary values as

$$A_1 + A_2 + \cdots + A_n = d_m 2^m + d_{m-1} 2^{m-1} + \cdots + d_1 2 + d_0,$$

where $A_i, d_i \in \{0, 1\}$ and the addition is the integer sum.

Various kinds of adders can be derived as special cases.

The arithmetic and Reed-Muller expressions are viewed as particular examples of Fourier series-like expressions over different fields, the complex field C and the Galois field $GF(2)$. These expressions are used to describe arithmetic circuits as adders and multipliers. The first publications on that subject Komamiya prepared in 1951 when he discussed the conversion of decimal to binary systems [4],

but it is reasonable to assume that he did a research on that subject earlier. Note that related approaches were promoted by Aiken and his research group, and this joint interests possibly explain the visit of Komamiya to the Computation Laboratory of Harvard University in 1957.

The theory of computing networks by Komamiya [6] was reviewed by Calvin C. Elgot, in *The Journal of Symbolic Logic*, Vol. 23, No. 3, 1958, 366.

The work of Komamiya presented in [6] was reported later also in [12] and pointed out in [13].

In [10], it is explicitly stated the relationship between the canonical sum-of-product expressions F for Boolean functions and their positive polarity Reed-Muller forms f in the following manner. If all logical OR symbols in F are replaced by exclusive-or symbols and if negated variables appearing in the fundamental product are omitted, the resulting expression is f. The constant term 1 will appear in f if there exists fundamental product $\overline{x}_1\overline{x}_2\overline{x}_3\cdots\overline{x}_n$.

Conversely, F can be obtained from f if exclusive-or symbols are replaced by logical OR symbols and if each product is multiplied by the missing variables, each in negated form. If there exists the constant term 1 in f, the fundamental product $\overline{x}_1\overline{x}_2\overline{x}_3\cdots\overline{x}_n$ should appear in F. So, it can be seen that F and f has an $1-1$ correspondence, where f is the Reed-Muller transform of F.

Another important and useful result in converting decimal to binary numbers is the observation that a decimal number $r_{10} = x_1+x_2+x_3+\cdots+x_n$, $x_i \in \{0,1\}$, can be expressed as $r_{10} = (y_k, y_{k-1}, y_{k-2}, \ldots, y_1, y_0)$, with $y_i = SB(n, 2^i)$, where $SB(n,k)$ are n-variable symmetric functions defined as the exclusive-or of all the products of binary variables x_i consisting of k literals, with by definition $SB(n,0) = 1$. Therefore, $SB(n,0) = 1$, $SB(n,1) = \bigoplus x_i$, $SB(n,2) = \bigoplus_{i<j} x_i x_j$, $SB(n,3) = \bigoplus_{i<j<k} x_i x_j x_k$, ..., and finally $SB(n,n) = x_1x_2x_3\cdots x_n$.

4 First Relay Computers in Japan

The work towards designing of a non stored-program computer working in the asynchronous mode started in November 1944 by Komamiya and Ryouta Suekane. The prototype was completed in 1952 and named by Prof. Mochinori Goto, the Director of ETL at that time, as ETL Mark I [17]. This prototype served as a pilot version for designing an entirely functional computer Mark II based on the same principles.

The team engaged in designing of ETL Mark I and ETL Mark II consisted of the following members of the Mathematical Research Group of ETL. Mochinori Goto, the Director of ETL, served as the Director of the Construction Committee, working at the same time as a Professor of the University of Tokyo. Yasuo Komamiya, the Chief of the Mathematics Research Group of ETL, served as the Chief Designer and the Sub-Director of the Construction Committee. Ryouta Suekane was a member of the Construction Committee and served as an Assistant Designer in charge for logical design. Masahide Takagi served as Assistant Designers in charge for circuit designs. Shigeru Kuwabara was another Assistant Designer. They all were members of the Mathematical Research Group of ETL.

To develop a fast, reliable and low-power machine, they specially designed three different types of relays as basic elements. The S type relay for storage: They are fast, have a few contacts, and low-power. The C type relay for control and arithmetic: They are fast, have many contacts, but high-power. The G type relay for gates: They have many contacts, low-power, but slow. In the combinational part, they used double-rail logic: Every bit is represented by a pair of signals $(A, \overline{A})$, which makes asynchronous self-checking operation possible. On the other hand, in the storage part, they used single-rail logic. The C type relay has main and holding coils, and works as a Set-Reset flip-flop. The ETL Mark II is the floating point parallel machine with 200 words consisting of 22,253 relays [11]. It was the largest and fastest relay computer in the world at that time.

Figure 2 shows the ETL Mark II computer exhibited in the National Museum of Nature and Science in Tokyo. ETL Mark II was built by Fuji Communication Apparatus Manufacturing Co. (now Fujitsu), while the company Shinko-Seisaku-Sho made the input equipment, i.e., tape readers and perforators. Mr. K. Noda, Chief of Electromagnetic Machinery Section of ETL designed motor generator for the power supply of the computer. Mr. T. Okabe Chief of the Temperature Control Research Group of ETL designed the air-conditioning process of the room where the computer was located [11].

The construction and functioning of Mark II was described with many details in the book *Theory and Structure of The Automatic Relay Computer ETL Mark II* by the designer staff of ETL. Final editing was done by Y. Komamiya and S. Kuwabara. This book was published by the ETL, Agency of Industrial Science and Technology, Japan, in the series *Researches of The Electrotechnical Laboratory* as the volume No. 556 and printed by the International Academic Printing Co., Ltd. (Kokusai Bunken Insatsusha) in Fujimi-cho, Chiyoda-ku, Tokyo, Japan for 500 samples in September 1956. This makes that in the antiquarian book shops its price presently achieves around USA $1,250.

In Synopsis of this book, Prof. Mochinori Goto wrote

Since the end of war, the Mathematics Research Group of Electrotechnical Laboratory has been studying logical mathematics, especially its applications to relay networks. As an outcome of this study, the theory of relay networks considering the time lag of switching elements was completed by one of the authors, M. Goto, and the theory of computing networks by Y. Komamiya in 1951. Applying the results of these studies, the Mathematical research Group have been engaged in the construction of the Plot Model of the automatic relay computer ETL Mark I completed in 1952, and subsequently have been engaged in the construction of the automatic relay computer ETL Mark II for practical use completed in November 1955. These computers, therefore, have been built on the same principles. The features of these computers are as follows. The computers are controlled without electric clock pulses, each relay being energized by its preceding relay in the same fashion as a row of falling nine-pins. As a result,

The calculating speed of the computers are 4 to 5 times as fast as any other relay computer, and

These computers perform self-checking simultaneously with calculation, if the

computer misses a calculation, the unit causing the trouble performs automatically the 2nd trial. Intermittent troubles are omitted automatically and the computer stops only in the event of an essential trouble. Therefore, there can be no trouble as long as the computers are running.
These features were developed from a new computer design based on our research in logical mathematics.

This book was review by Calvin C. Elgot in *The Journal of Symbolic Logic*, Vol. 23, No. 1, 1958, 60.

In 1956, the cost of the ETL Mark II was about Japanese 36,000,000 Yen or about USA $100,000. The exchange rate of 1.00 USA $ was about 360.00 Yen. For a comparison the salary of a bank worker who just graduate a university was 10,000 Yen per month at that time.

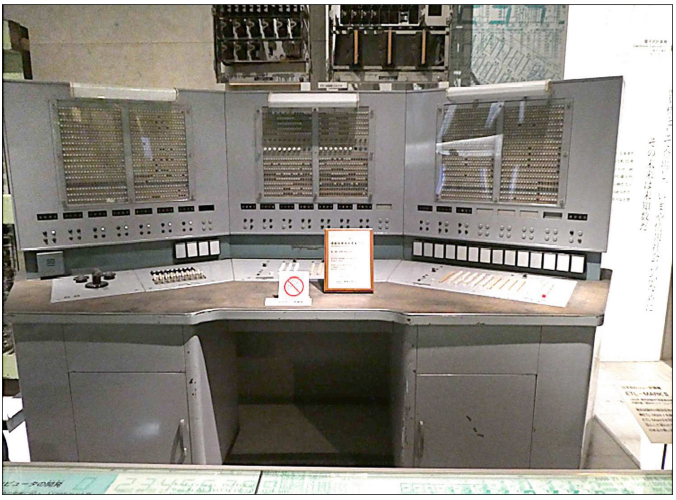

Fig. 2. The ETL Mark II relay computer, photo by T. Sasao.

5 Summary of the Work on First Computers in Japan

In this section, we give a brief summary of the development of first computers in Japan. For more details, we refer to [18].

Transistor was invented at Bell Laboratories in 1948. However, at that time ETL people could not research on transistors formally. They started an informal study in a series of meetings on transistors. Electrical Communication Laboratory succeeded in manufacturing germanium transistors in 1951.

As Electrical Communication Laboratory became a part of the public corporation in 1952, ETL established Electronics Department in it in 1954 and started the research on transistors and transistor computers formally.

Eiichi Goto invented Parametron in 1954. Then, Electrical Communication Laboratory decided to develop Parametron computers. Notice that at that time

the reliability of transistors was low while parametrons were more reliable and less expensive. ETL developed ETL Mark III transistor computer using point-contact transistors in July, 1956. This is the first transistor computer in Japan. Electrical Communication Laboratory developed the first Parametron computer MUSASINO-1 in March 1957.

Figure 3 shows a photo of Eiichi Goto (seating) and Hidetoshi Takahasi. Recall that a parametron is a resonant circuit containing a non-linear reactive element which oscillates at half the driving frequency.

ETL developed ETL Mark IV transistor computer using junction-type transistors in November, 1957. Hidetoshi Takahasi and Eiichi Goto of University of Tokyo developed another Parametron computer PC-1 in March, 1958. This is a binary, single-address computer with magnetic core memory. Later the advantage was given to transistor computers mainly because of the speed. Several commercial transistor computers were developed based on first ETL transistor computers [18]. Moreover, Dr. Mochinori Goto, General Director of ETL named the ETL's first transistor computer as ETL Mark III following the relay computers ETL Mark I and Mark II which Dr. Komamiya developed. Recently, there is a renewed interest in basic principles of parametron devices related to quantum computing and also nanomechanical computers. *D-Wave Systems* from Canada adopted superconductivity quantum bits (qubits) and quantum annealing system. To amplify magnetic flux, they introduced the quantum flux Parametron invented by Eiichi Goto in 1986. Quantum annealing system was proposed by Prof. Nishimori of Tokyo Institute of Technology, who was awarded NEC C&C Prize on Nov. 28, 2018. It might be said that the combination of quantum flux parametron and quantum annealing system created a new quantum computer. Nanomechanical computers based on the principle of parametron were proposed in 2008 at the NTT Research Labs in Kanagawa.

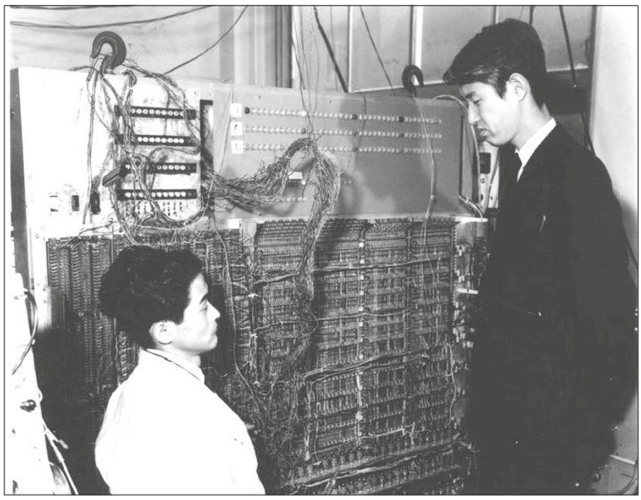

Fig. 3. Eiichi Goto (seating) and Hidetoshi Takahasi.

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