Karnaugh Maps

With

A Brief History of Logic Design

by

Jon T. Butler

Naval Postgraduate School

Monterey, CA U.S.A.


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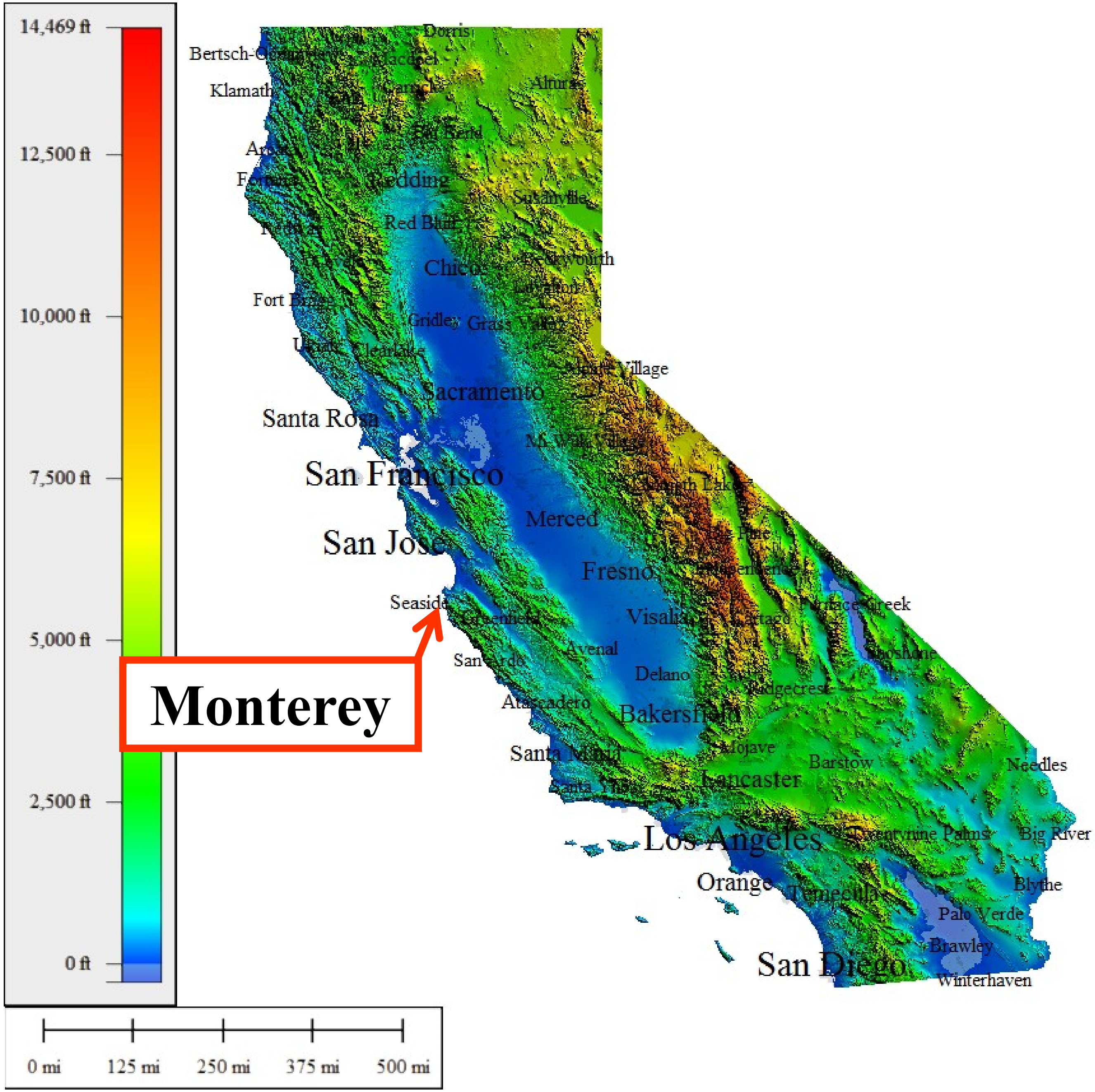
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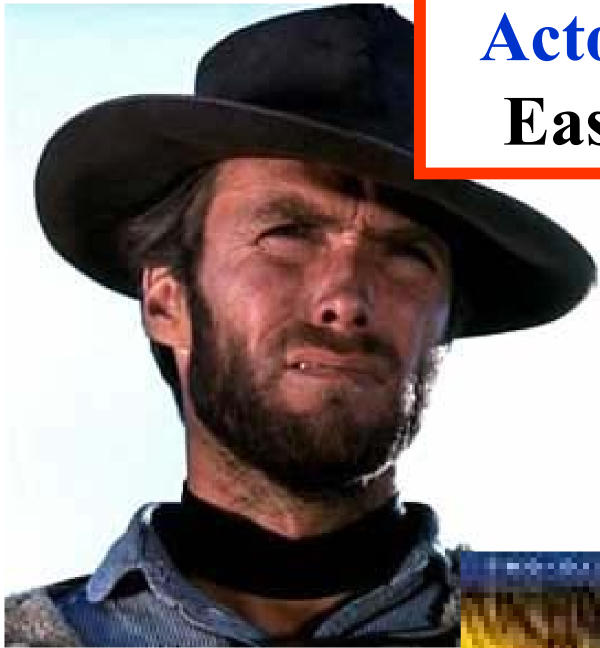

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A Brief History of Logic Design

Functions of a Logic Variable

Much of what we study here dates back to the work of George Boole (1815-1864), who established the mathematics of logic in *An investigation of the laws of thought* published in 1854. Boole died in 1864 after walking from home to school in the rain and lecturing in wet clothes. He was 49 years old. Boole's work was not used until Charles S. Peirce (1839-1914) who was the first to consider its application to electronic circuits.

From http://en.wikipedia.org/wiki/George_Boole

Functions of a Logic Variable

Claude E. Shannon (1916 - 2001) was born in Petoskey, Michigan. His father was a businessman and his mother was a language teacher. He graduated in 1940 from MIT with a Master's degree in electrical engineering and a Ph.D. degree in mathematics. His Master's thesis was *A Symbolic Analysis of Relay and Switching Circuits*. This was based on Boole's theory and laid the foundation for switching theory used in today's computers.

From http://en.wikipedia.org/wiki/Claude_Shannon

Functions of a Logic Variable

1932: Entered Univ. of Michigan at 16.

1936: Graduated from Univ. of Michigan with an EE and a Math. undergraduate degree at 20.

1937: Completed masters thesis on switching theory at 21.

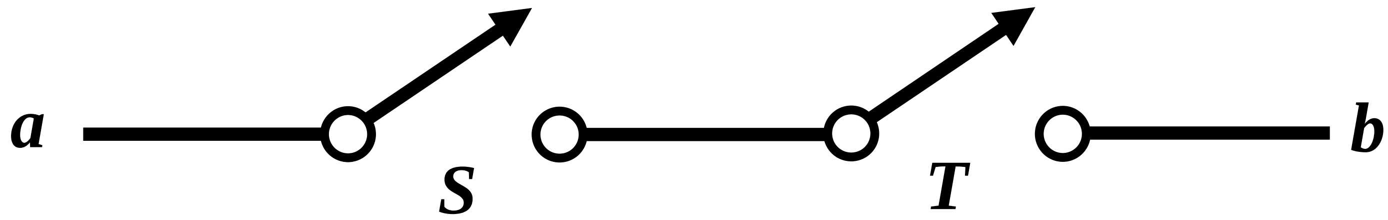
1938: Published "A symbolic analysis of relay and switching circuits" in *AIEE Transactions* at 22.

Later, Shannon established information theory.

From http://en.wikipedia.org/wiki/Claude_Shannon

Functions of a Logic Variable

Because they were used for telephone exchanges and for motor control, Shannon studied two-terminal switching circuits, like that shown below

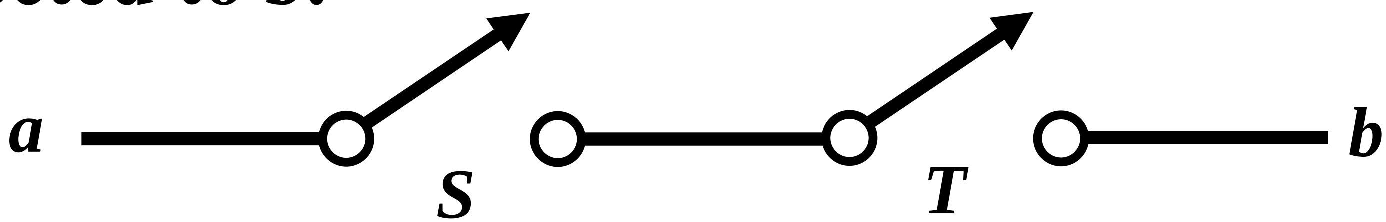


Is this series connection more like

1. **AND ($S\ T$) or**
2. **OR ($S + T$) ?**

Functions of a Logic Variable

It depends whether you focus on the conditions when 1. *a* is connected to *b* or 2. *a* is not connected to *b*.

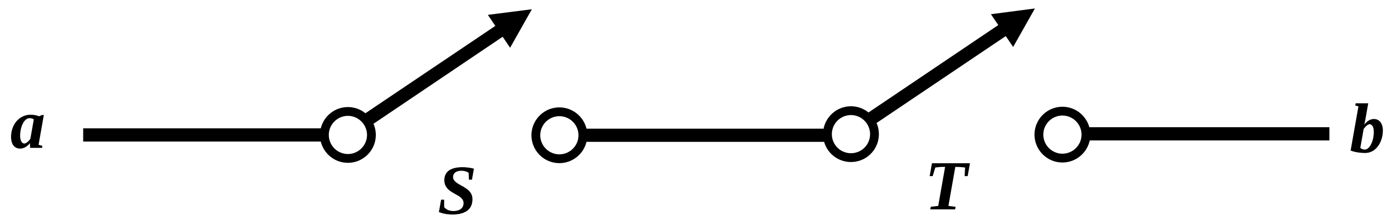


If you focus on the conditions when *a* is connected to *b*, then this occurs when *S* AND *T* are connected.

If you focus on the conditions when *a* is not connected to *b*, then this occurs when *S* OR *T* are not connected. Shannon adopted this viewpoint.

Functions of a Logic Variable

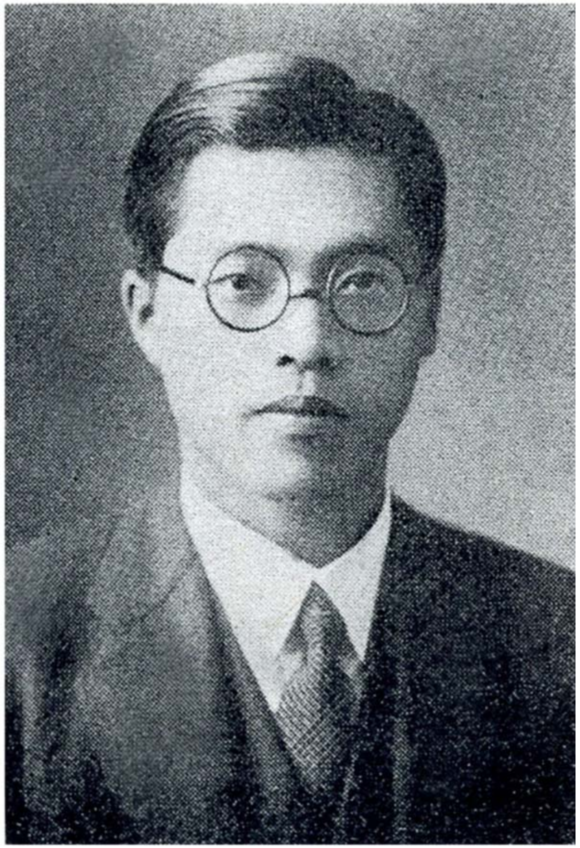
It is interesting that the foundation of computing lies on the theory of two-terminal circuits that are nowadays very old technology



However, there is a surprise. Shannon was not the first to establish switching theory.

Functions of a Logic Variable

Akira Nakashima of NEC published a series of papers on switching theory between 1934 and 1938 all of which were <u>*before*</u> Shannon's publications.



From Akihiko Yamada.

Nakashima was born in 1908 and graduated from University of Tokyo in 1930 at 22. At NEC, he initially worked on switching circuits, but in 1936 at 26 was transferred to the transmission engineering group. However, he

Functions of a Logic Variable

continued to work on switching theory at night. Nakashima’s contributions continued until 1941. Later, Nakashima served as managing director of NEC and was appointed president of Ando Electric Co. in 1965 until be died in 1970 at 62 [1].

Nakashima’s writings are considered difficult to read (even for Japanese*). On the other hand, Shannon was considered to be a lucid writer.

*** The Japanese written language changed considerably.**

Functions of a Logic Variable

	Title(translation)	Publication	English version	Contents	Referenced by
1	Theory and Practice of Relay Circuit Engineering	Nichiden Geppo (Nippon Electric), Vol. 11, No.11, 1934.11, - Vol.12, No. 9, 1935.9	-	Definitions of relays, contact point types of relays and analysis of transient phenomena	
2	Transient Phenomena During Releasing Operation of a Relay With Two Parallel Coils	Nichiden Geppo (Nippon Electric), Vol.12, No.4, 1935.4	-	Analysis of transient phenomena	
3	The Theory of Relay Circuit Composition	J. I. T. T. E. J., No. 150, 1935.9	1936.5	Relay circuit categorization, duality and de Morgan's theory	
4	Approximation Solution of the Transient Phenomena During the Operating and Releasing Action of Telephone Relays Having Many Varied Secondary Circuits	J. I. T. T. E. J., No. 152, 1935.11	-	Analysis of transient phenomena	
5	On Reziprozitaetsgesetze	Nichiden Geppo (Nippon Electric), Vol.13, No.1, 1936.1	-	Reziprozitaetsgesetze	
6	Some Properties of the Group of Simple Partial Paths	J. I. T. T. E. J., No. 155, 1936.2	1937.3	Application of group theory	
7*	A. Nakashima and M. Hanzawa: "The Theory of Equivalent Transformation of Simple Partial Paths in the Relay Circuit (Part I),"	J.I.T.T.E., No. 165, 1936.12	1938.2	Distribution law, elimination law, serial-parallel transformation and algebraic expression	H. Piesch
8*	The Theory of Equivalent Transformation of Simple Partial Paths in the Relay Circuit (Part II),"	J.I.T.T.E., No. 167, 1937.2			

Functions of a Logic Variable

9	The Theory of Four-Terminal Passive Networks in Relay Circuits	J.I.T.T.E., No. 169, 1937.4	1938.4	The theory of four-terminal passive networks in relay circuits	C.E. Shannon
10	Algebraic Expressions Relative to Simple Partial Paths in the Relay Circuits	J. IECE J., 1937.8	1938.9	Interpretation based on group theory and principle of dual circuits	C.E. Shannon
11	The Theory of Two-Point Impedance of Passive Networks in the Relay Circuits (Part I)	J. IECE J., 1937.12	1938.11	Law of development of impedance functions and the theory of designing two terminal networks in the relay circuits	C.E. Shannon
12	The Theory of Two-Point Impedance of Passive Networks in the Relay Circuits (Part II)	J. IECE J., 1938.1			
13	The Transfer Impedance of Four-Terminal Passive Networks in Relay Circuits	J. IECE J., 1938.2	1938.12	The transfer impedance of four-terminal passive networks	
14*	Expansion Theorem and Design of Two-Terminal Networks in Relay Networks (Part 1),	J. IECE J., No. 206, 1940.5	1941.4	Expansion theorem and design of two-terminal networks	
15*	Expansion Theorem and Design of Two-Terminal Networks in Relay Networks (Part 2)	J. IECE J., No. 206, 1940.8	1941.10		
16	Theory of Relay Circuits	J. IECE J, 1947.7	-	A panoptic paper of Nakashima's research on switching theory	

Note: * Co-authored with Masao Hanzawa , ** Published in Nippon Electrical Communication Engineering

J.I.T.T.E.J.: Journal of the Institute of Telegraph and Telephone Engineers of Japan

J.I.ECE.J.: Journal of the Institute Electrical Communication Engineers of Japan

This table is from [1].

Functions of a Logic Variable

There are five known statues of Shannon – 1. Univ. of Michigan, 2. MIT, 3. Gaylord, MI, 4. AT&T Bell Labs, and 5. U.C.-San Diego.

From http://www.eecs.umich.edu/shannonstatue/

[1] A. Yamada, "History of research on switching theory in Japan – On the contributions of Akira Nakashima," ***Proceedings of the Reed-Muller Workshop 2009, Naha, Okinawa, May 23-24, 2009, pp. 1-7.***

Karnaugh Maps

Minimizing Logic Circuits

GOAL: Find the minimal realization of the function

A	*B*	*C*	*f*(*A*,*B*,*C*)	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	0	
1	0	0	0	
1	0	1	0	
1	1	0	1	$AB\overline{C}$
1	1	1	1	ABC

Minimizing Logic Circuits (cont'd)

Algebraic Solution:

Write a canonical sum-of-products expression

$$f(A,B,C) = AB\overline{C} + ABC$$

Apply distributivity **OR**

$$f(A,B,C) = AB(\overline{C} + C)$$

Apply $\overline{C} + C = 1$ **and** $AB1 = AB$

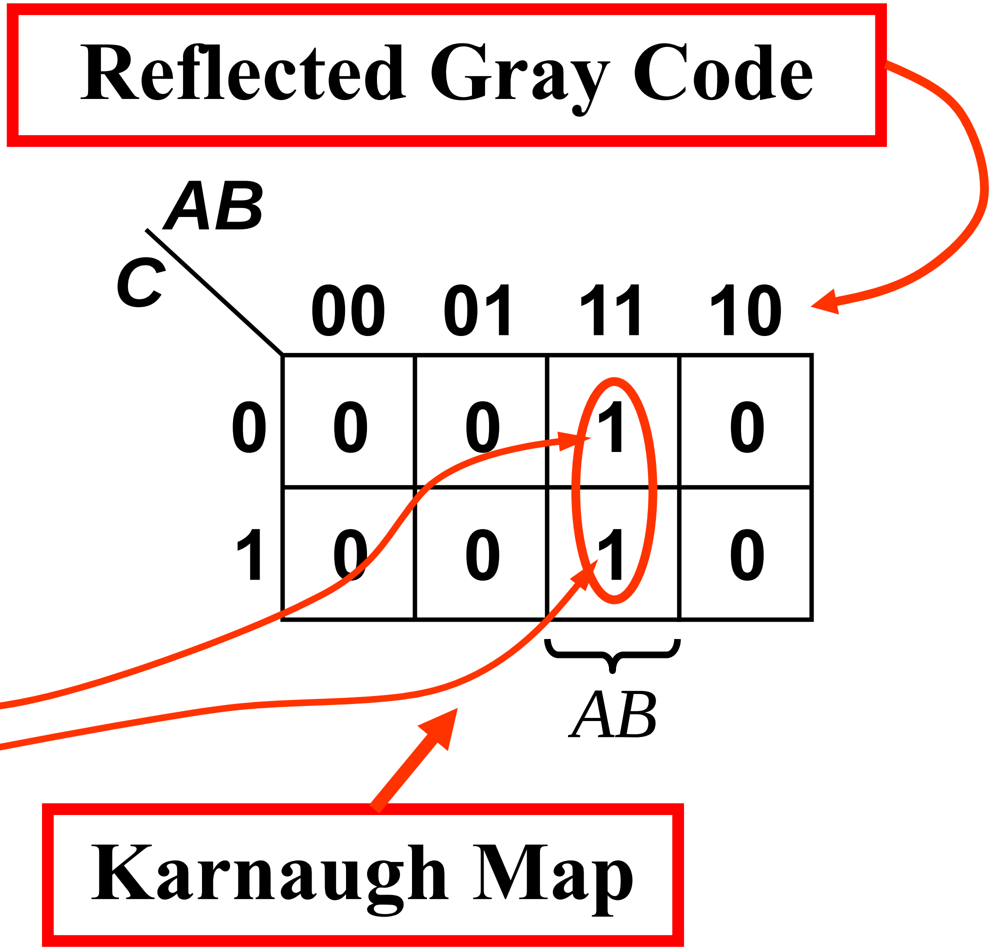
$$f(A,B,C) = AB$$

Needs one 2-input AND gate.

Minimizing Logic Circuits (cont'd)

<u>GOAL</u>: Find the AND-OR two-level minimal realization of the function (Find the minimum SOP.)

A	*B*	*C*	*f*(*A*,*B*,*C*)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



Minimizing Logic Circuits (cont'd)

Karnaugh Map Solution:

Circle the two adjacent pair of 1's and write the corresponding expression

$$f\left(A,B,C\right) = AB$$

Karnaugh Maps are an easy way to do algebra

Minimizing Logic Circuits (cont'd)

Karnaugh Maps were developed by Maurice Karnaugh, a Bell Laboratories engineer in 1953 and presented as

Maurice Karnaugh, "The map method for synthesis of combinational logic circuits," *Transactions of the American Institute of Electrical Engineers*, 72, 1, 593-599, November, 1953

Maurice Karnaugh

Maurice Karnaugh was born on October 24, 1924 in New York City. He studied mathematics and physics at City College of New York (1944-1948) . He transferred to Yale University and received his B.Sc. Degree in 1949, M.Sc. in 1950, and his Ph.D. in physics in 1952 (in magnetic resonance)

In 1992, he published "Generalized quicksearch for expert systems" in *Proc. Artificial Intelligence for applications*, pp. 30-34, 1992.

Minimizing Logic Circuits (cont'd)

GOAL: Find the AND-OR two-level minimal realization of the function

A	*B*	*C*	*f*(*A*,*B*,*C*)	
0	0	0	0	
0	0	1	0	
0	1	0	0	
0	1	1	0	
1	0	0	0	
1	0	1	1	$A\bar{B}C$
1	1	0	1	$AB\bar{C}$
1	1	1	1	ABC

Minimizing Logic Circuits (cont'd)

Algebraic Solution:

Write a canonical sum-of-products expression

$$f\left(A,B,C\right)=A\overline{B}C+ABC+AB\overline{C}$$

Apply $ABC = ABC + ABC$

$$f\left(A,B,C\right)=A\overline{B}C+ABC+ABC+AB\overline{C}$$

Apply distributivity

$$f\left(A,B,C\right)=\left(B+\overline{B}\right)AC+AB\left(C+\overline{C}\right)$$

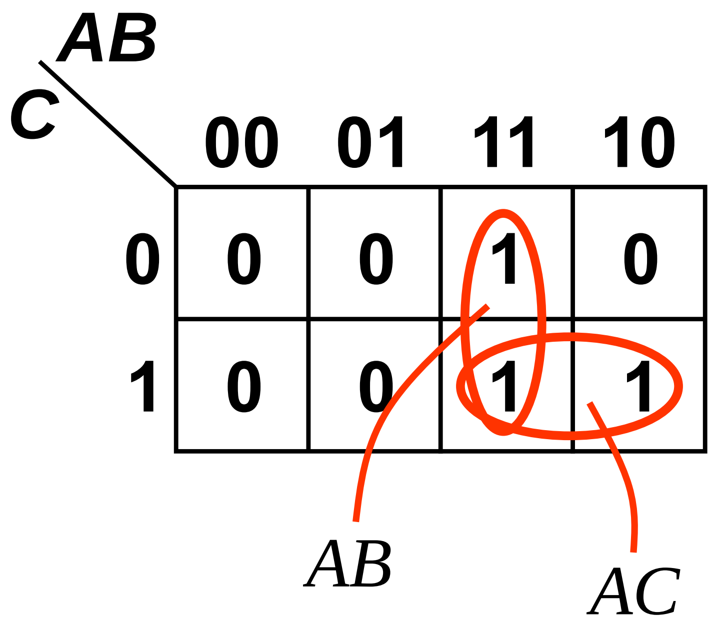
Apply $B+\overline{B}=1$ **and** $A1C = AC$

$$f\left(A,B,C\right)=AC+AB$$

Minimizing Logic Circuits (cont'd)

GOAL: Find the AND-OR two-level minimal realization of the function

A	*B*	*C*	*f*(*A*,*B*,*C*)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1



Minimizing Logic Circuits (cont'd)

Karnaugh Map Solution:

Circle the two adjacent pairs of 1's and write the corresponding expression

$$f\left(A, B, C\right) = AB + AC$$

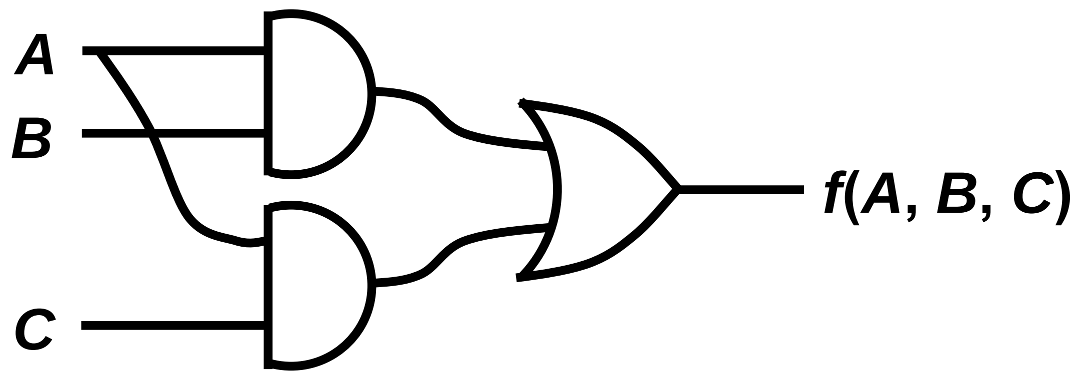
Karnaugh Maps are an easy way to do algebra

Minimizing Logic Circuits (cont'd)

Minimal AND-OR two-level circuits are not necessarily minimal. Consider

$$f(A, B, C) = AB + AC$$

which can be realized as

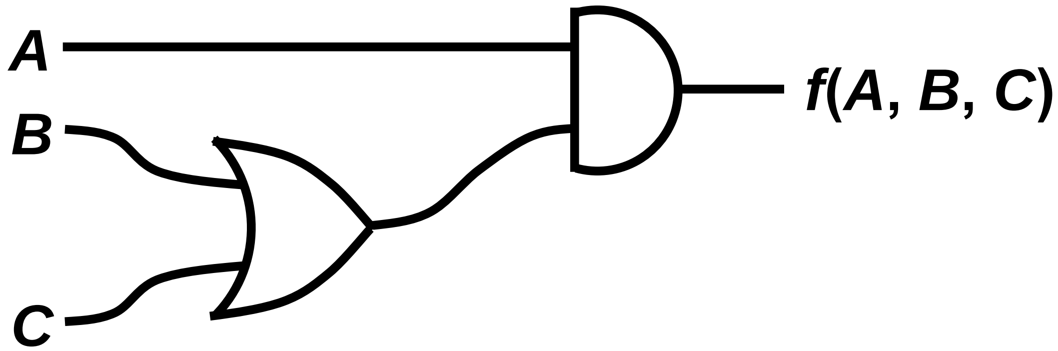


Minimizing Logic Circuits (cont'd)

However, we can write

$$f\left(A,B,C\right)=AB+AC=A\left(B+C\right)$$

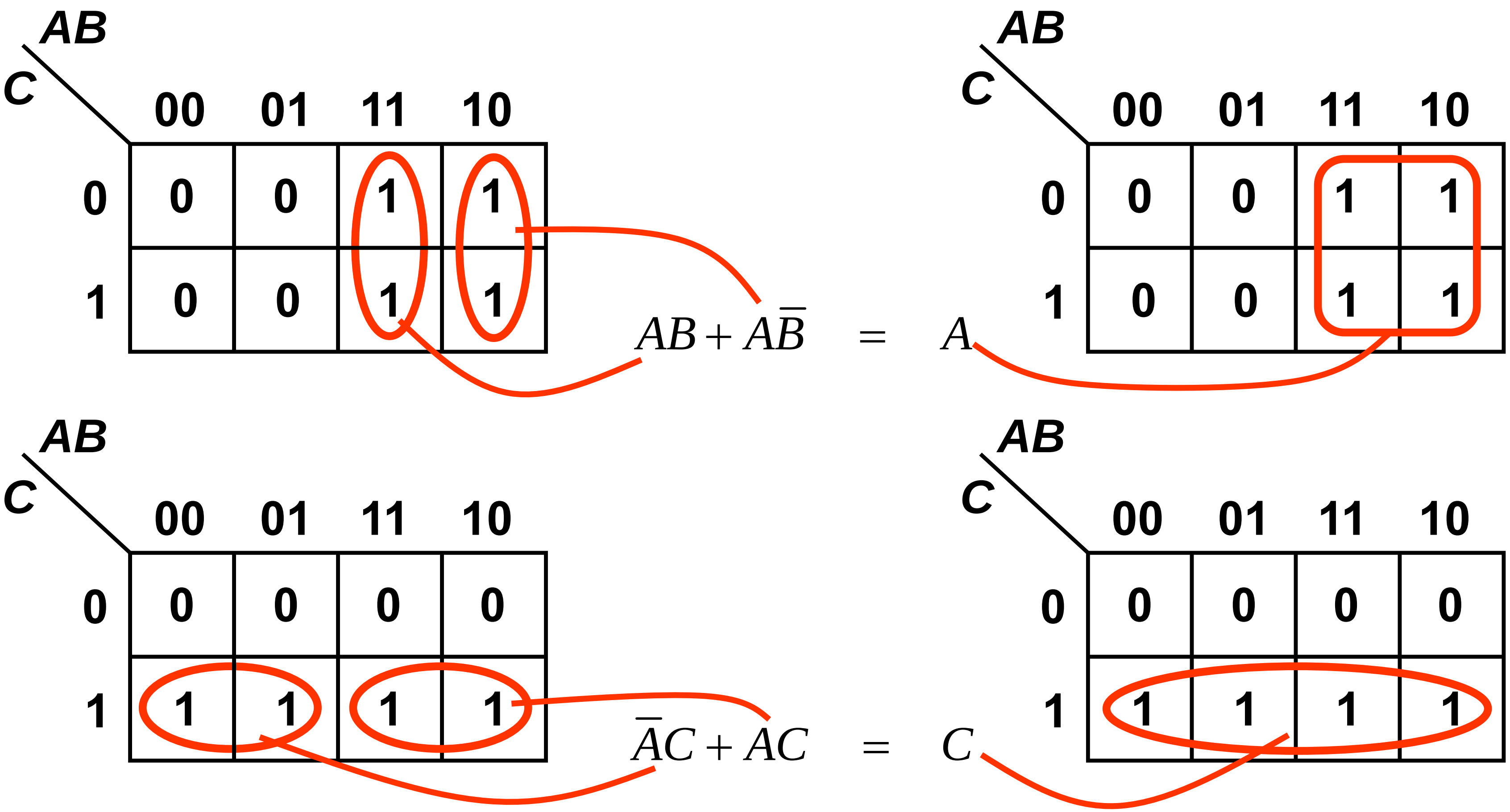
which can be realized as



This is NOT an AND-OR two-level circuit. Rather, it is an OR-AND two-level circuit.

Other Combinations

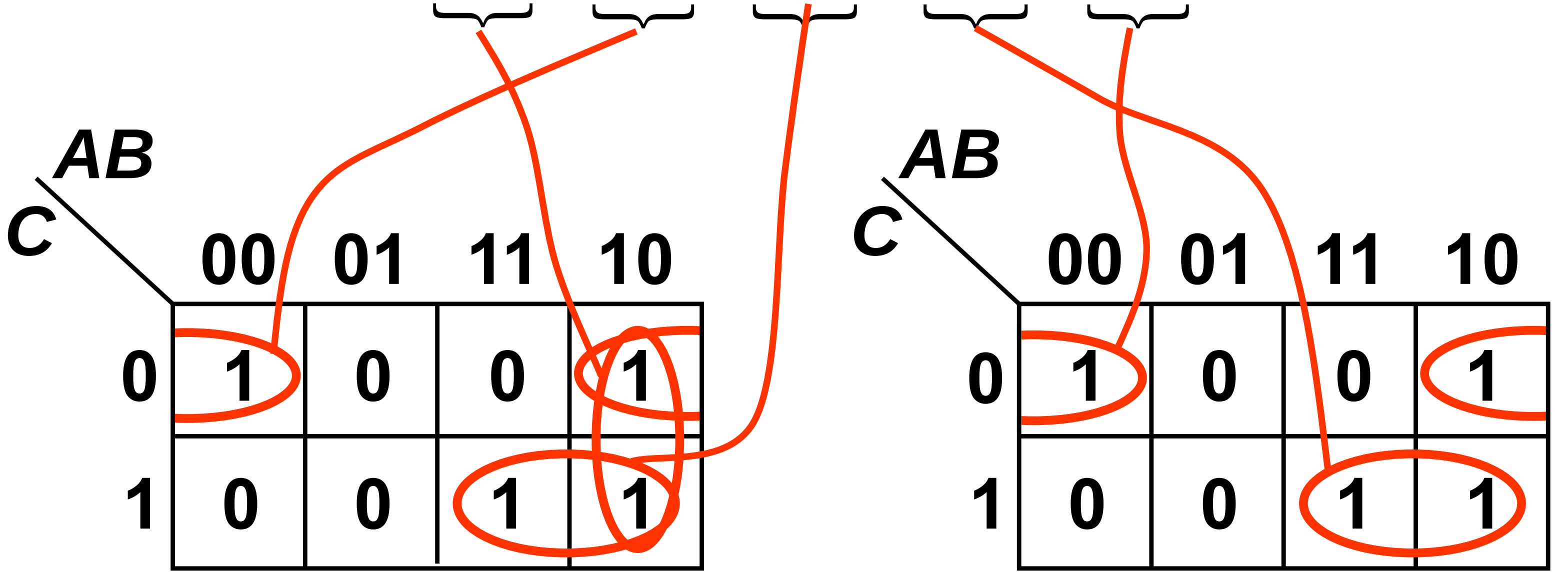
From previous slides, a pair of 1's yields a single product term. However, other combinations are possible.



A “Look-See” Proof of Consensus

Use the Karnaugh Map to prove a result stated previously. This is called “consensus”.

$$\underbrace{A\bar{B}} + \underbrace{\bar{B}\bar{C}} + \underbrace{AC} = \underbrace{AC} + \underbrace{\bar{B}\bar{C}}$$



Other Examples

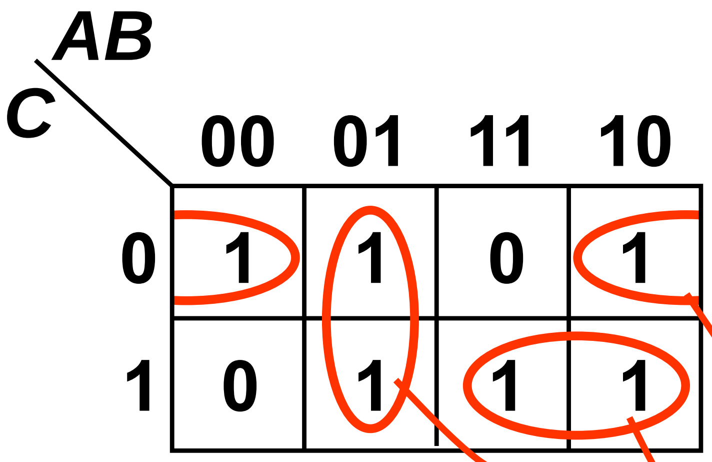
C \ AB	00	01	11	10
0	0	0	0	0
1	1	0	1	1

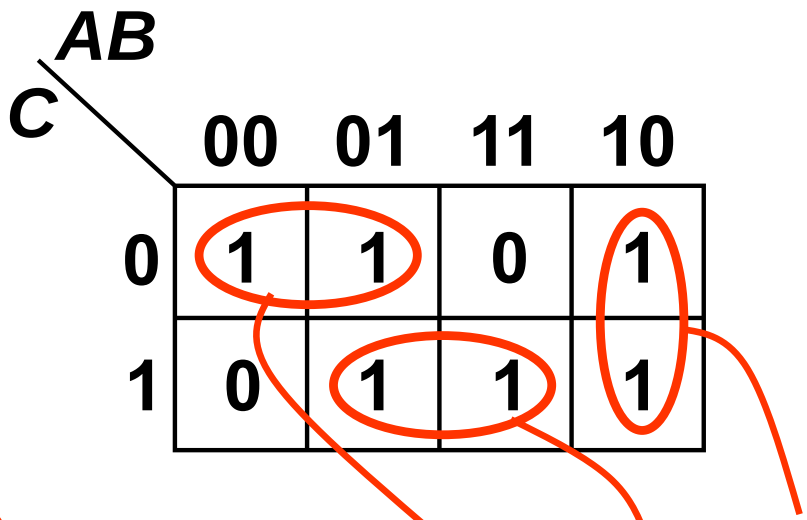
$$f\left(A,B,C\right)=\overline{B}C+AC$$

C \ AB	00	01	11	10
0	1	1	1	0
1	1	1	0	0

$$f\left(A,B,C\right)=\overline{A}+B\overline{C}$$

Other Examples (cont'd)





$$f(A,B,C) = \bar{B}\bar{C} + \bar{A}B + AC \qquad f(A,B,C) = \bar{A}\bar{C} + BC + A\bar{B}$$

Procedure for Karnaugh Map Circling

1. **Start by covering single 1 cells that cannot combine with any other 1 cell. Circle 1 cells that can combine in only one way with one other 1 cell. Continue: circle 1's that combine uniquely in a group of 4, 8, 16, etc.**

2. **A minimal expression is obtained as a collection of 1's that are as large as possible and as few as possible, so that every 1 cell is covered.**

Four-Variable Karnaugh Map

CD \ AB	00	01	11	10
00	0	0	1	1
01	1	0	0	0
11	0	1	1	0
10	1	1	1	1

$$f(A,B,C,D) = \bar{A}\bar{B}\bar{C}D + A\bar{D} + BC + C\bar{D}$$

CD \ AB	00	01	11	10
00	0	0	1	0
01	1	1	1	0
11	0	1	1	1
10	0	1	0	0

$$f(A,B,C,D) = AB\bar{C} + \bar{A}\bar{C}D + \bar{A}BC + ACD$$

Four-Variable Karnaugh Map (cont'd)

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	1	1	0
11	0	0	1	1
10	0	1	1	0

$$f\left(A,B,C,D\right) = A\overline{C}\overline{D} + B\overline{C}D + ACD + BC\overline{D}$$

Forbidden Circlings

CD \ AB	00	01	11	10
00	0	1	1	1
01	0	0	0	0
11	1	0	0	0
10	0	1	0	0

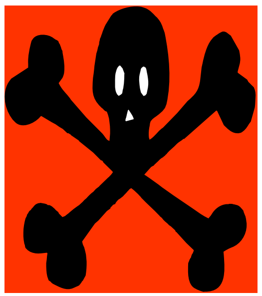
$$\bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$$

$$B\bar{C}\bar{D} \quad + \quad A\bar{C}\bar{D}$$

Not combinable

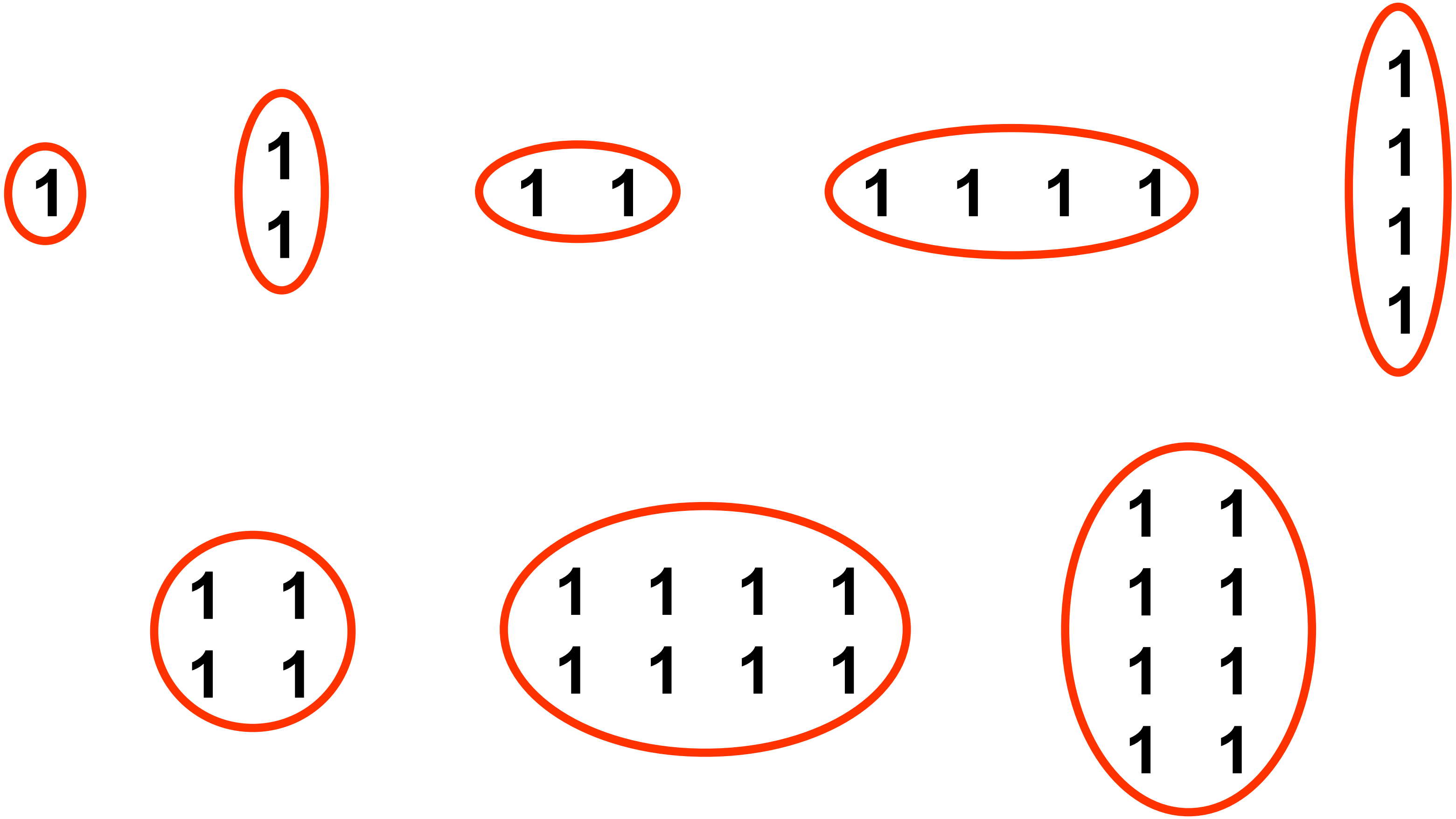
$$\bar{A}\bar{B}CD + \bar{A}BC\bar{D}$$

Not combinable



Warning !

Acceptable Circlings



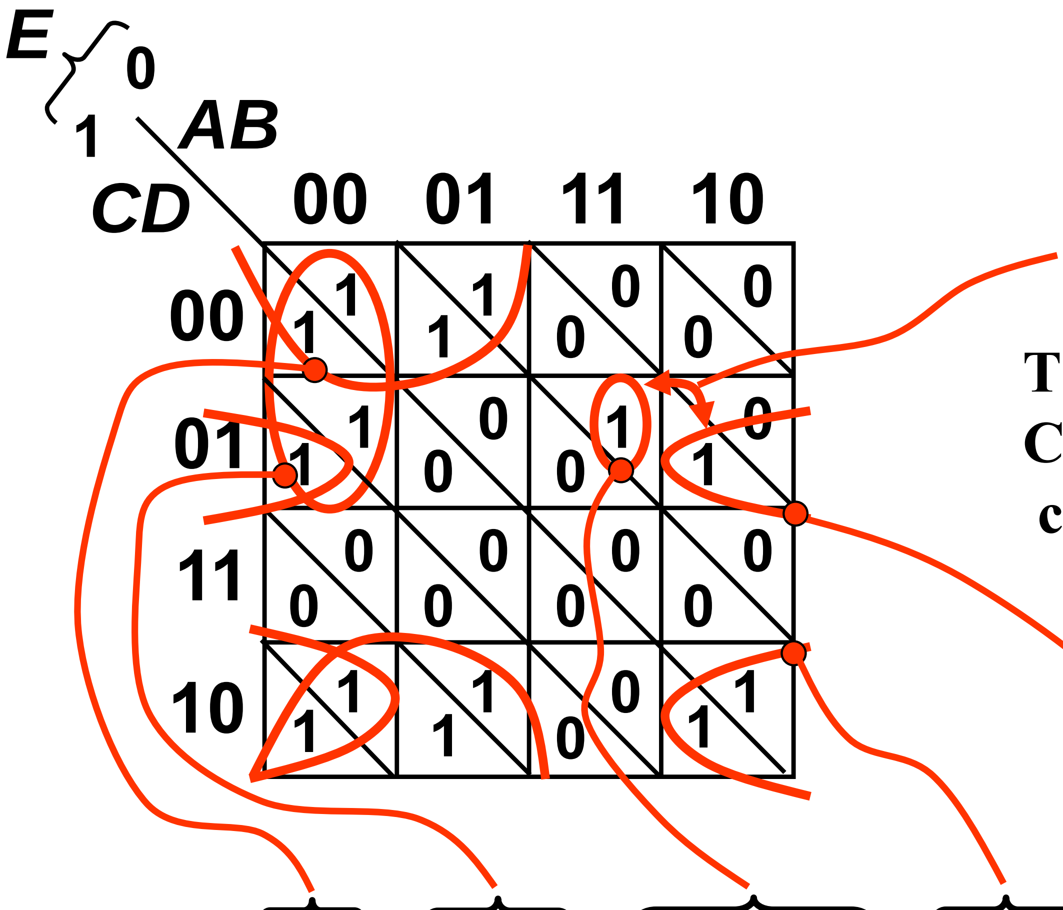
Five-Variable Karnaugh Map

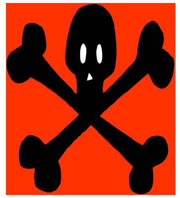
Reflected Gray Code

DE \ ABC	000	001	011	010	110	111	101	100
00	1	0	0	0	0	0	0	0
01	0	1	0	0	0	0	1	0
11	0	0	0	0	0	0	0	0
10	1	0	0	1	1	1	1	0

$$f\left(A,B,C,D,E\right)=\bar{A}\bar{B}\bar{C}\bar{E}+\bar{B}C\bar{D}E+B\bar{C}D\bar{E}+ACD\bar{E}$$

Five-Variable Karnaugh Map



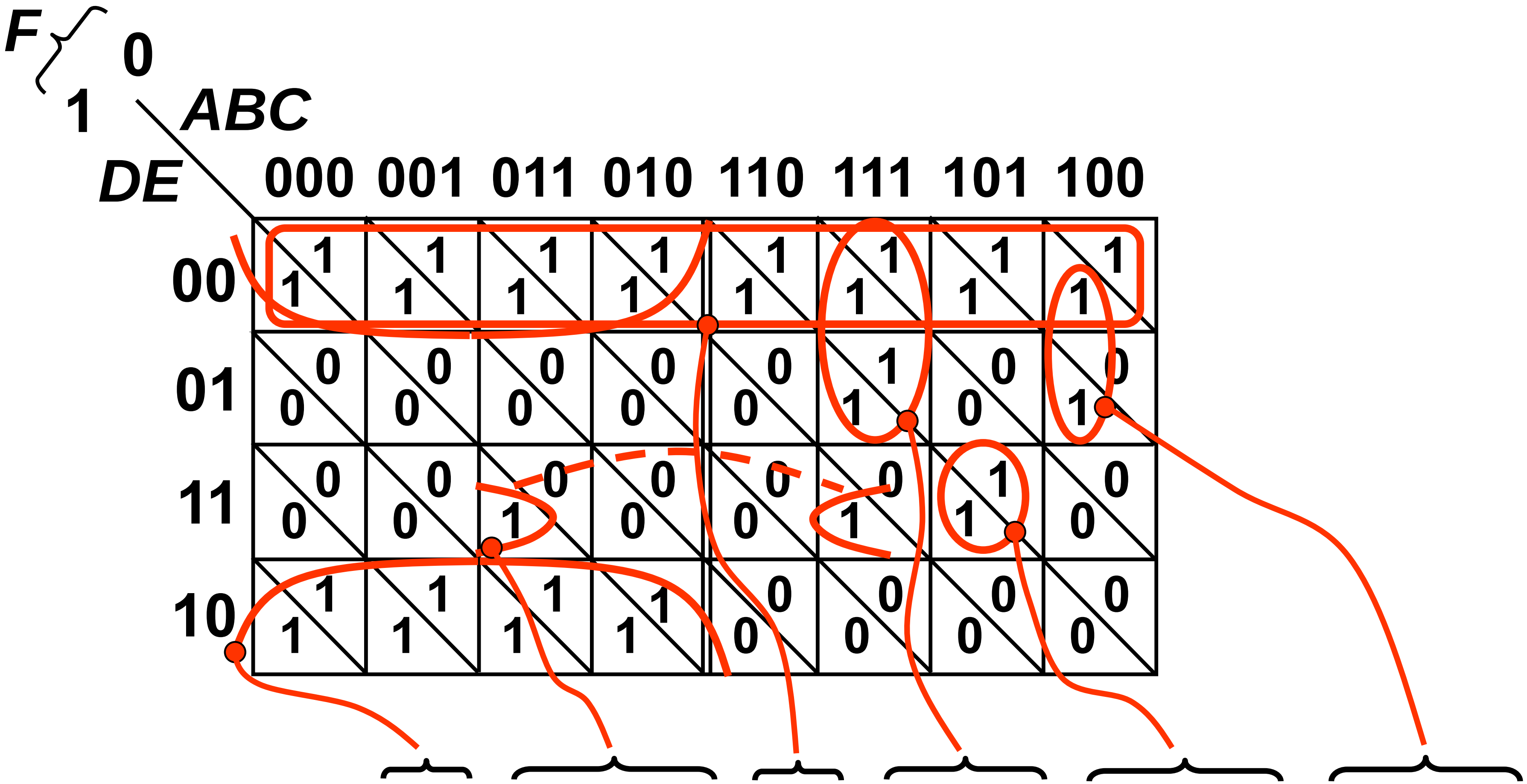


Warning !

This pair of 1's CANNOT be combined.

$$f(A,B,C,D,E) = \overbrace{\bar{A}\bar{D}} + \overbrace{\bar{A}\bar{B}\bar{C}} + \overbrace{AB\bar{C}D\bar{E}} + \overbrace{\bar{B}C\bar{D}} + \overbrace{\bar{B}\bar{C}DE}$$

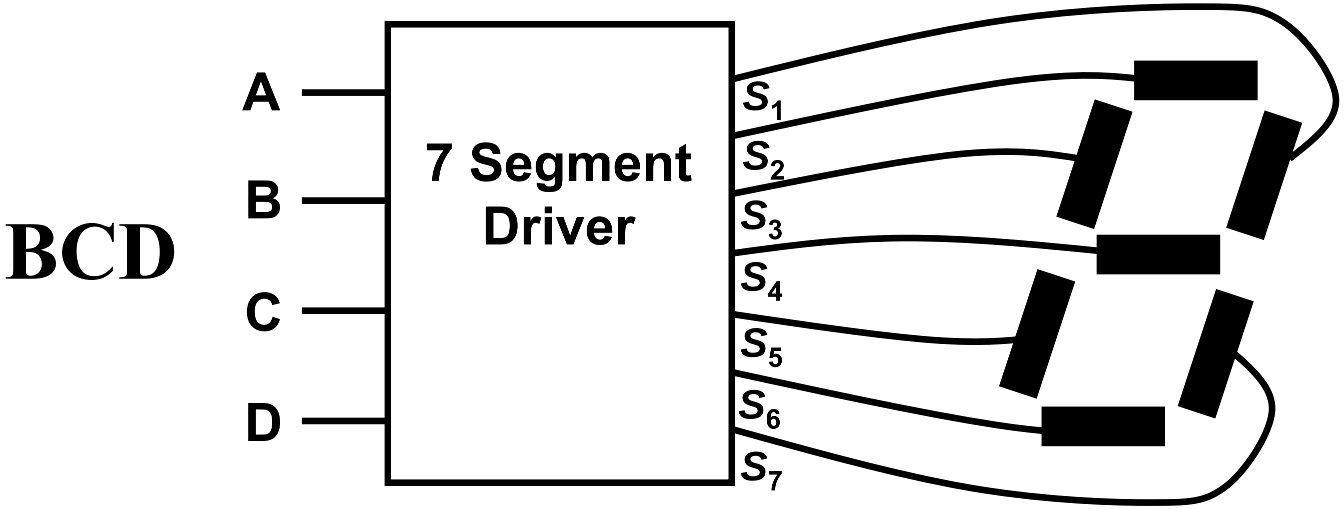
Six-Variable Karnaugh Map



$$f\left(A,B,C,D,E,F\right)=\overline{A}\,\overline{E}+BCDEF+\overline{D}\,\overline{E}+ABC\overline{D}+A\overline{B}CDE+A\overline{B}\,\overline{C}\,\overline{D}F$$

Don’t Care Values

Don’t care values result when certain assignments of values to variables never occur. For example,



The designer can expect that the assignments *ABCD* = 1010, 1011, …, 1111 will never occur. Thus, S_1, S_2, …, and S_7 take on don’t care values for these assignments.

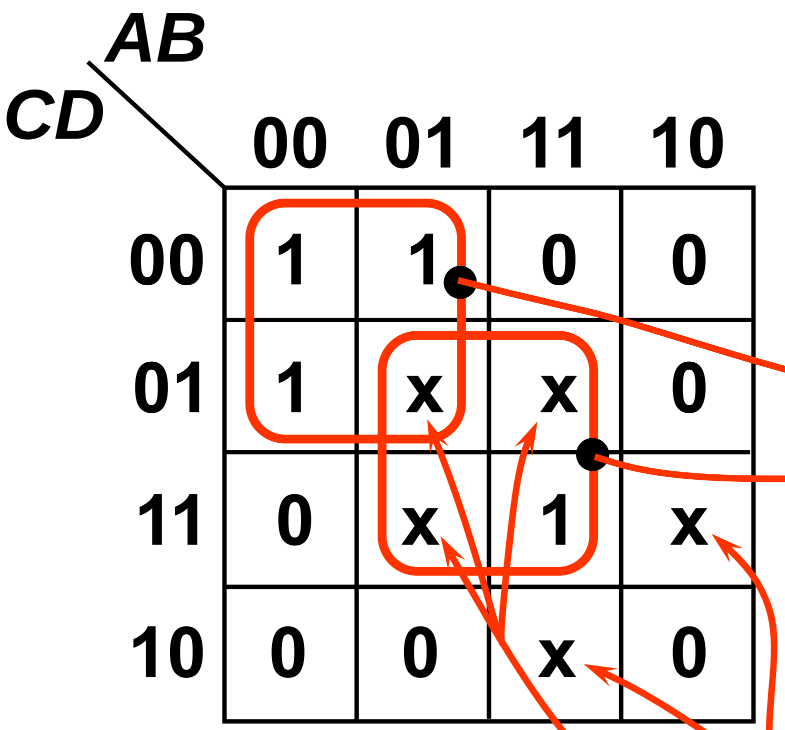
Minimizing an Expression with Don’t Cares

Two Approaches

1. Find the minimal circuit for each assignment of values to the don’t cares (choose each don’t care as 0 or 1). If there are *k* don’t cares, there are 2^k functions (not practical for large *k*).

2. Enter don’t cares into Karnaugh Map and select the fewest largest circles.

Example of Approach #2



$$f(A,B,C,D) = \bar{A}\bar{C} + BD$$

This solution "chooses" **these don't care values as 0 and these don't care values as 1.**

Two Problems

CD \ AB	00	01	11	10
00	x	x	1	0
01	0	1	x	1
11	x	x	x	x
10	x	0	x	x

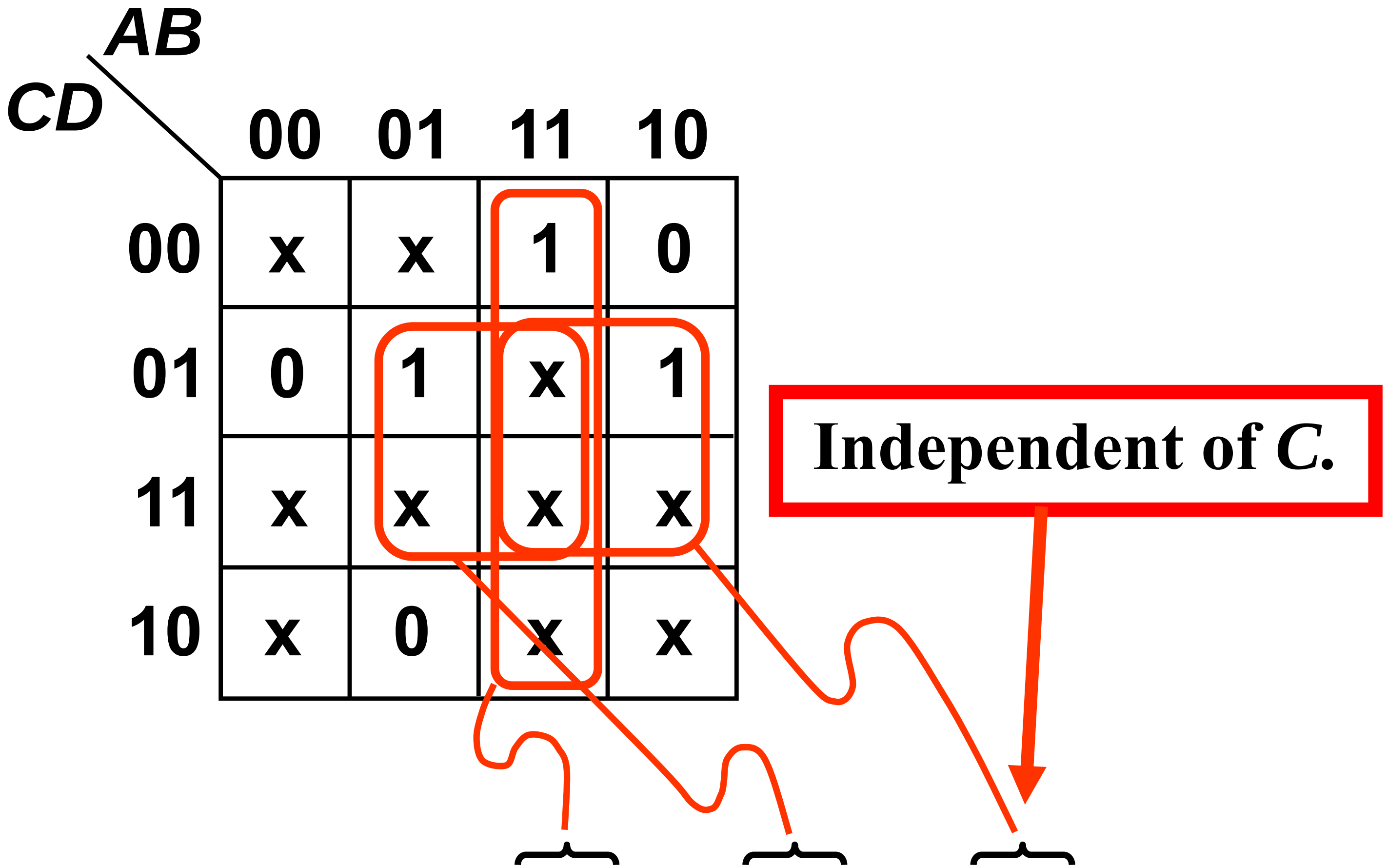
1. **Minimize number of product terms**
2. **Minimize number of dependent variables.**

Minimize number of product terms

CD \ AB	00	01	11	10
00	x	x	1	0
01	0	1	x	1
11	x	x	x	x
10	x	0	x	x

$$f(A,B,C,D) = \overbrace{B\overline{C}} + \overbrace{AD}$$

Minimize number of dependent variables



$$f(A,B,C,D) = \overbrace{AB} + \overbrace{BD} + \overbrace{AD}$$

Minimizing a Circuit with Don't Cares

Two Problems

1. Minimize the number of product terms allows for smaller AND-OR circuits. Our example minimized to 4 variables and 2 product terms. It is useful in ordinary circuits.

2. Minimize the number of dependent variables allows for smaller memory. Our example minimized to 3 variables, so that it is useful for PLA designs.

Short Quiz

1. $x_1 + \overline{x_1} = 1$ True/False

2. $x_1 + 1 = x_1$ True/False

3. $x_1+x_2+x_3$ has a minimum sum-of-products expression with 3 product terms. True/False

4. I understood everything the teacher said today. True/False

5. There are 3 false statements here. True/False

Can you find them?

Short Quiz

1. This statement is false. **True/False**

Thank you